THAT WHICH IS CLAIMED IS:

1. A semiconductor device comprising:

an interlayer dielectric layer disposed on a semiconductor substrate;

a buried contact plug extending a distance through the interlayer dielectric to be in electrical communication with a predetermined region of the semiconductor substrate;

an oxidation barrier pattern disposed on a top surface of the buried contact plug; and

a lower electrode disposed on the oxidation barrier pattern,

wherein a top surface area of the oxidation barrier pattern is substantially equal to a bottom surface area of the lower electrode.

2. The semiconductor device of claim 1, wherein the oxidation barrier pattern comprises conductive metal nitride.

3. The semiconductor device of claim 1, wherein the lower electrode comprises a noble metal and/or a conductive compound containing a noble metal.

4. The semiconductor device of claim 1, wherein the lower electrode includes an external sidewall and the oxidation barrier pattern includes a sidewall, and wherein the lower electrode external sidewall and the oxidation barrier pattern sidewall are aligned in a substantially straight line.

5. The semiconductor device of claim 1, further comprising:

an upper electrode disposed over the lower electrode; and

a dielectric film interposed between the lower electrode and the upper electrode to thereby provide a capacitor.

6. The semiconductor device of claim 5, wherein the dielectric film is made of a material having a higher dielectric constant than oxide-nitride-oxide (ONO).

7. The semiconductor device of claim 5, wherein the dielectric film comprises a ferroelectric substance.

8. The semiconductor device of claim 5, wherein the upper electrode is made of at least one noble metal and/or a conductive compound containing a noble metal.

9. The semiconductor device of claim 1, in combination with a transistor connected to the oxidation barrier pattern to provide a memory cell.

10. A method for fabricating a semiconductor device, comprising:

forming an oxidation barrier pattern and a capping layer pattern which are sequentially stacked on a semiconductor substrate;

encasing exposed surfaces of the capping layer pattern with a mold insulating layer so that the mold insulating layer extends a distance above the capping layer pattern and between adjacent capping layer patterns, the mold insulating layer material having an etch selectivity with respect to the capping layer pattern material;

planarizing the mold insulating layer until a top portion of the capping layer pattern is exposed;

removing the capping layer pattern to form a lower electrode recess exposing substantially an entire top surface of the corresponding underlying oxidation barrier pattern; and

forming a lower electrode about inner surfaces of the lower electrode recess,

wherein the capping layer pattern is made of a material having an etch selectivity with respect to the oxidation barrier pattern material.

11. The method of claim 10, wherein before formation of the oxidation barrier pattern and the capping insulating layer pattern onto the semiconductor substrate, the method comprises:

disposing an interlayer dielectric and an etch-stop layer over the semiconductor substrate so that the interlayer dielectric is closer the semiconductor substrate; and

positioning a buried contact plug so that the contact plug extends through the etch-stop layer and the interlayer dielectric film to be in electrical communication with a predetermined region of the semiconductor substrate,

wherein a top surface of the buried contact plug is adapted to contact a

predetermined region of a bottom side of the oxidation barrier pattern, and wherein the etch-stop layer is made of an insulating material having an etch selectivity with respect to the mold insulating layer material.

12. The method of claim 10, wherein the oxidation barrier pattern comprises conductive metal nitride.

13. The method of claim 10, wherein the capping layer pattern comprises silicon nitride.

14. The method of claim 10, wherein the mold insulating layer comprises silicon oxide.

15. The method of claim 10, wherein the formation of the lower electrode comprises:

conformably forming a lower electrode layer on an exposed portion of the stacked semiconductor substrate including the inner surfaces of the lower electrode recess;

forming a sacrificial insulating layer on the lower electrode layer to fill the lower electrode recess; and

planarizing the sacrificial insulating layer and the lower electrode layer down to a top portion of the mold insulating layer to form a lower electrode in the lower electrode recess.

16. The method of claim 10, wherein the lower electrode comprises at least one noble metal and/or conductive compound containing a noble metal.

17. The method of claim 16, after formation of the lower electrode, the method further comprises:

etching the molding insulating layer to be removed; and

sequentially stacking a dielectric film and an upper electrode on an upper surface of the lower electrode.

18. The method of claim 17, wherein the dielectric film has a higher

dielectric constant than oxide-nitride-oxide (ONO).

19. The method of claim 17, wherein the dielectric film comprises a ferroelectric substance.

20. The method of claim 17, wherein the upper electrode comprises a noble metal and/or a conductive compound containing a noble metal.

21. A MIM capacitor comprising:

an upper electrode;

a lower electrode; and

a dielectric layer interposed therebetween,

wherein the lower electrode has a bottom and at least one sidewall, the bottom being disposed over an oxidation barrier pattern that defines a lower electrode platform with a top surface, wherein the oxidation barrier pattern resides above and is in electrical communication with a region of a semiconductor substrate, and wherein the lower electrode bottom has a surface area that is substantially coextensive with the surface area of the top surface of the platform defined by the oxidation barrier pattern.

22. A capacitor according to Claim 21, wherein the dielectric layer is a dielectric film having a dielectric constant that is greater than that of oxide-nitride-oxide.

23. A capacitor according to Claim 22, wherein the capacitor resides in a unit cell of an integrated circuit DRAM memory device.

24. A capacitor according to Claim 21, wherein the dielectric layer is a ferroelectric film.

25. A capacitor according to Claim 21, wherein the capacitor is in a unit cell of a ferroelectric memory device.

26. A semiconductor device having a plurality of capacitors of a metal-insulator-metal structure, the capacitors each including upper electrodes, lower

electrodes and a dielectric layer interposed therebetween, with the capacitors residing above a semiconductor substrate with each capacitor having a corresponding oxidation barrier pattern in electrical communication with respective regions of the semiconductor substrate, wherein the device is configured so that the lower electrodes have a bottom surface area that is substantially equal to the surface area of the upper surface of the underlying oxidation barrier pattern.

27. A semiconductor device according to Claim 26, wherein the lower electrode is substantially cylindrical with a closed continuous surface bottom.

28. A semiconductor device according to Claim 26, wherein the dielectric layer has a dielectric constant that is greater than that of oxide-nitride-oxide.

29. A semi conductor device according to Claim 28, wherein the capacitor defines part of a unit cell of a DRAM memory device.

30. A semiconductor device according to Claim 26, wherein the dielectric layer is a ferroelectric material.

31. A semiconductor device according to Claim 30, wherein the capacitor defines part of a unit cell of a ferroelectric memory device.

32. A method for fabricating a semiconductor device with a plurality of MIM capacitors in unit cells of an integrated circuit memory device, comprising:

forming an oxidation barrier pattern on a semiconductor substrate; and

forming a lower electrode disposed on the oxidation barrier pattern so that a top surface area of the oxidation barrier pattern is substantially equal to a bottom surface area of the lower electrode.

33. A method according to Claim 32, wherein the lower electrode forming step comprises:

forming a layer on the oxidation barrier pattern, the layer having a recess with a bottom that is sized to be substantially coextensive with a top surface of the oxidation barrier pattern; and

applying a conductive layer in the recess to thereby form the lower electrode.

34. A method according to Claim 32, further comprising:

forming a interlayer dielectric layer on the semiconductor substrate prior to forming the oxidation barrier pattern; and

placinga contact plug in the interlayer dielectric layer so that it extends a distance through the interlayer dielectric to be in electrical communication with a predetermined region of the semiconductor substrate prior to forming the oxidation barrier pattern.

35. A method according to Claim 33, wherein the forming the layer onto the oxidation barrier pattern is carried out by applying a capping layer over the oxidation barrier pattern after the step of forming the oxidation barrier pattern, forming a capping layer pattern by selectively removing portions of the capping layer, disposing a mold insulating layer over the capping layer pattern and then removing the capping layer pattern to form the recess.